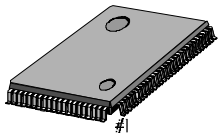
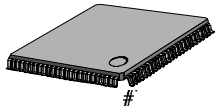
INTRODUCTION

The KS0108B is a LCD driver LSI with 64 channel output for dot matrix liquid crystal graphic display systems.
This device consists of the display RAM, 64 bit data latch, 64 bit drivers and decoder logics.
It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data.
The KS0108B composed of the liquid crystal display system in combination with the KS0107B (64 channel common driver).

100 QFP-1420C



100 TQFP-1414



FEATURES

- Dot matrix LCD segment driver with 64 channel output
- Input and Output signal
  - Input: 8 bit parallel display data
    Control signal from MPU
    Divided bias voltage (V0R, V0L, V2R, V2L, V3R, V3L, V5R, V5L)
  - Output: 64 channel for LCD driving.
- Display data is stored in display data RAM from MPU.
- Interface RAM
  - Capacity: 512 bytes (4096 bits)
  - RAM bit data: RAM bit data = 1: ON
    RAM bit data = 0: OFF
- Applicable LCD duty: 1/32 ~1/64
- LCD driving voltage: 8V ~17V(V_{DD}-V_{EE})
- Power supply voltage: + 5V ± 10%
- Interface

Driver		Controller
COMMON	SEGMENT	
KS0107B	Other KS0108B	MPU

- High voltage CMOS process.
- 100QFP / 100TQFP and bare chip available.

BLOCK DIAGRAM

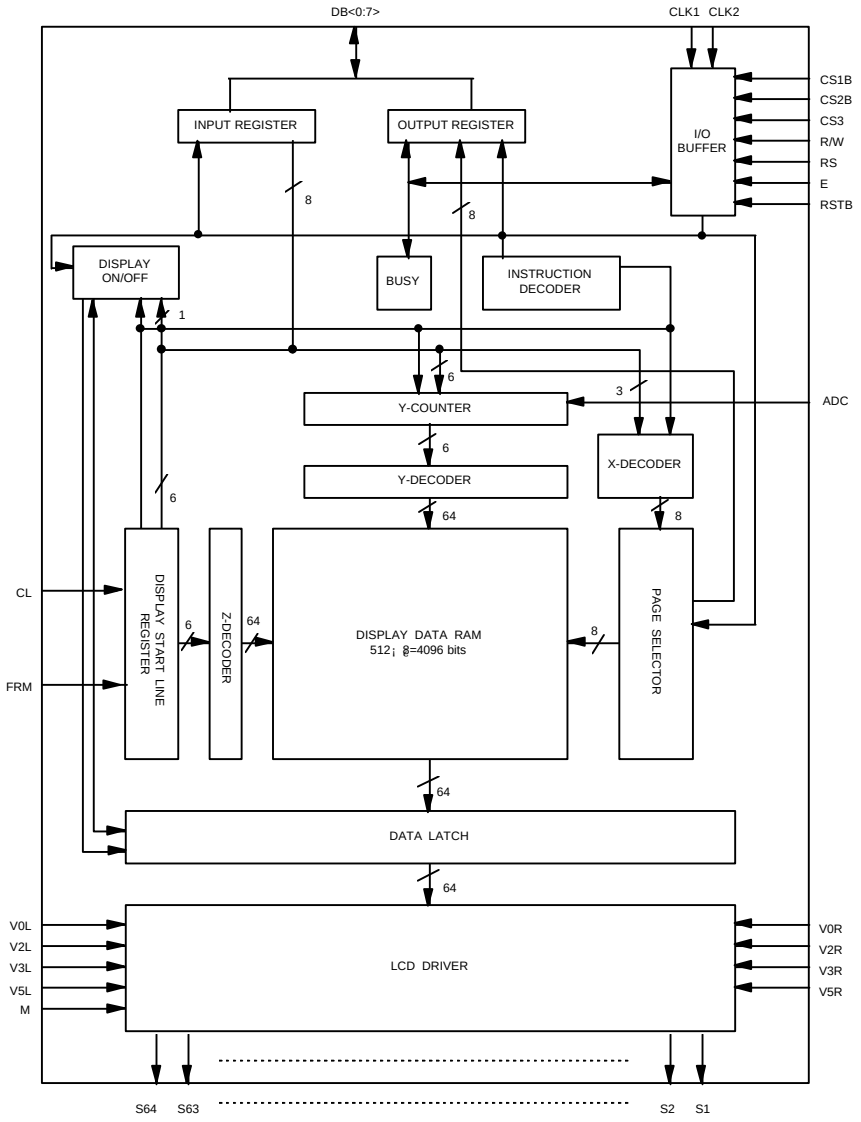


Fig1. KS0108B Functional block diagram

PIN CONFIGURATION

1. 100QFP

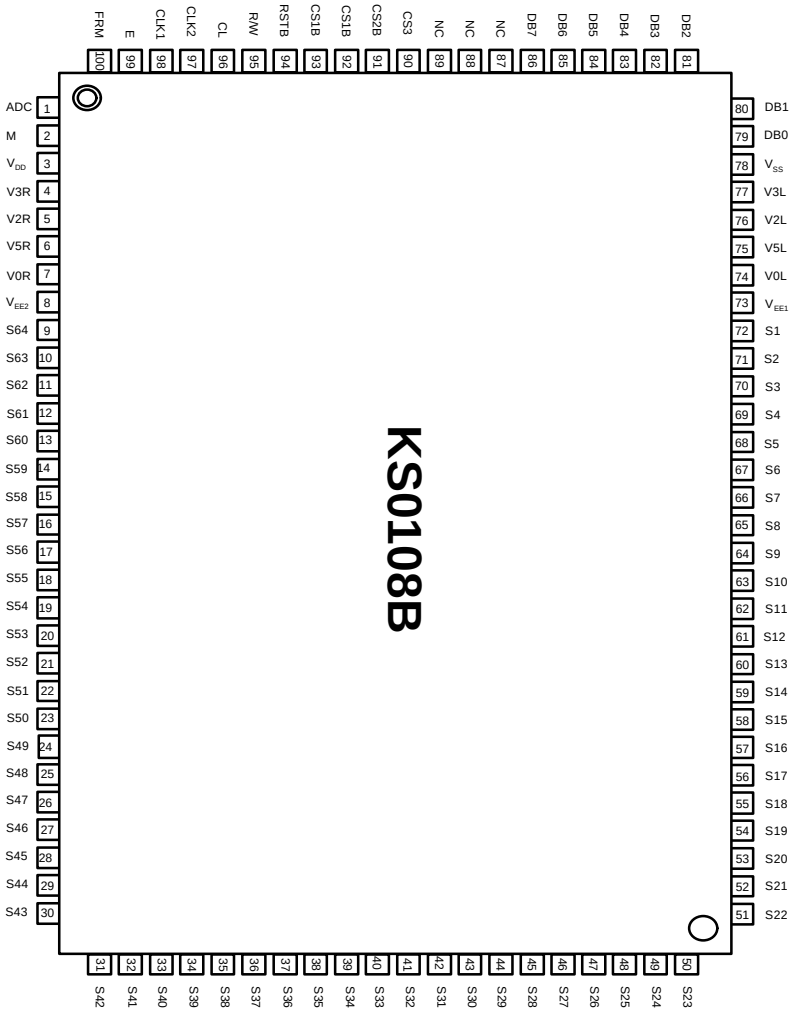
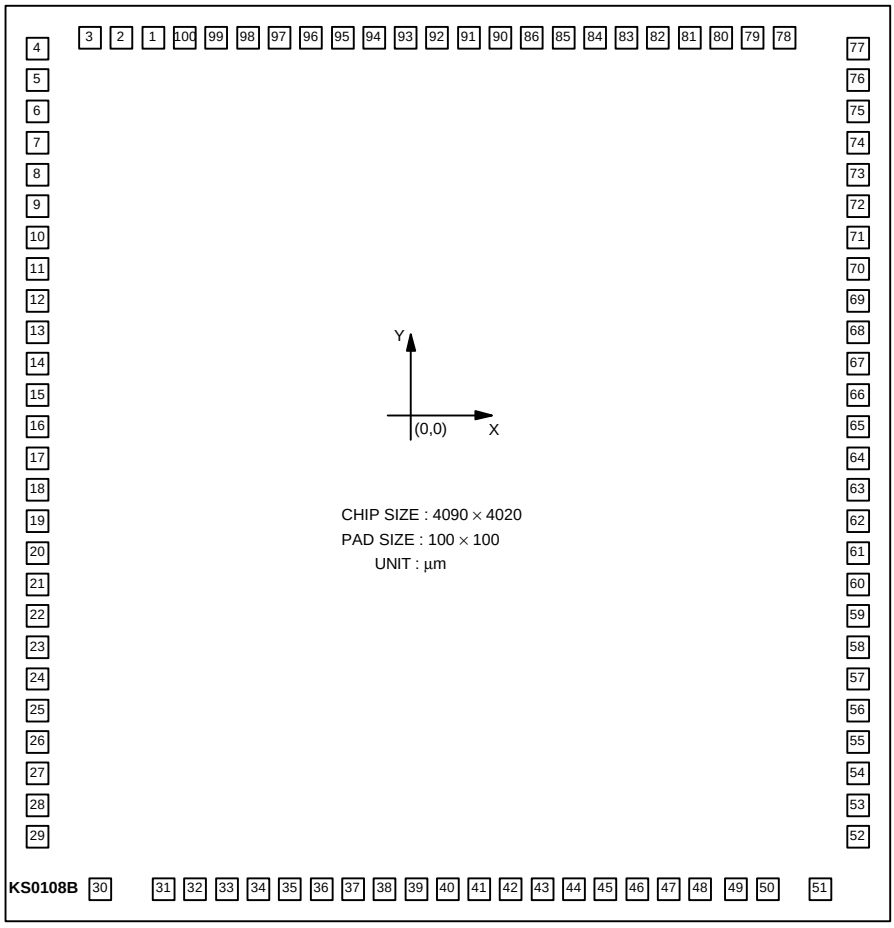


Fig2. 100QFP Top View

PAD DIAGRAM (Chip Layout for the 100QFP)



* There is mark of “KS0108B” on the bottom left in the chip.

PAD LOCATION (100QFP)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
1	ADC	-1140	1845	35	S38	-687	-1845	69	S4	1882	791
2	M	-1275	1845	36	S37	-562	-1845	70	S3	1882	916
3	VDD	-1410	1845	37	S36	-437	-1845	71	S2	1882	1041
4	V3R	-1882	1809	38	S35	-312	-1845	72	S1	1882	1166
5	V2R	-1882	1684	39	S34	-187	-1845	73	VEE1	1882	1310
6	V5R	-1882	1559	40	S33	-62	-1845	74	V0L	1882	1435
7	V0R	-1882	1434	41	S32	62	-1845	75	V5L	1882	1559
8	VEE2	-1882	1309	42	S31	187	-1845	76	V2L	1882	1684
9	S64	-1882	1165	43	S30	312	-1845	77	V3L	1882	1809
10	S63	-1882	1040	44	S29	437	-1845	78	VSS	1412	1845
11	S62	-1882	915	45	S28	562	-1845	79	DB0	1277	1845
12	S61	-1882	790	46	S27	687	-1845	80	DB1	1142	1845
13	S60	-1882	665	47	S26	812	-1845	81	DB2	1007	1845
14	S59	-1882	540	48	S25	937	-1845	82	DB3	882	1845
15	S58	-1882	415	49	S24	1062	-1845	83	DB4	757	1845
16	S57	-1882	290	50	S23	1187	-1845	84	DB5	632	1845
17	S56	-1882	165	51	S22	1487	-1845	85	DB6	507	1845
18	S55	-1882	40	52	S21	1882	-1379	86	DB7	382	1845
19	S54	-1882	-84	53	S20	1882	-1239	87	NC		
20	S53	-1882	-209	54	S19	1882	-1099	88	NC		
21	S52	-1882	-334	55	S18	1882	-959	89	NC		
22	S51	-1882	-459	56	S17	1882	-834	90	CS3	245	1845
23	S50	-1882	-584	57	S16	1882	-709	91	CS2B	120	1845
24	S49	-1882	-709	58	S15	1882	-584	92	CS1B	-5	1845
25	S48	-1882	-834	59	S14	1882	-459	93	RSTB	-130	1845
26	S47	-1882	-959	60	S13	1882	-334	94	R/W	-255	1845
27	S46	-1882	-1099	61	S12	1882	-209	95	RS	-380	1845
28	S45	-1882	-1239	62	S11	1882	-84	96	CL	-505	1845
29	S44	-1882	-1379	63	S10	1882	41	97	CLK2	-630	1845
30	S43	-1487	-1845	64	S9	1882	166	98	CLK1	-755	1845
31	S42	-1187	-1845	65	S8	1882	291	99	E	-880	1845
32	S41	-1062	-1845	66	S7	1882	416	100	FRM	-1005	1845
33	S40	-937	-1845	67	S6	1882	541				
34	S39	-812	-1845	68	S5	1882	666				

2. 100TQFP

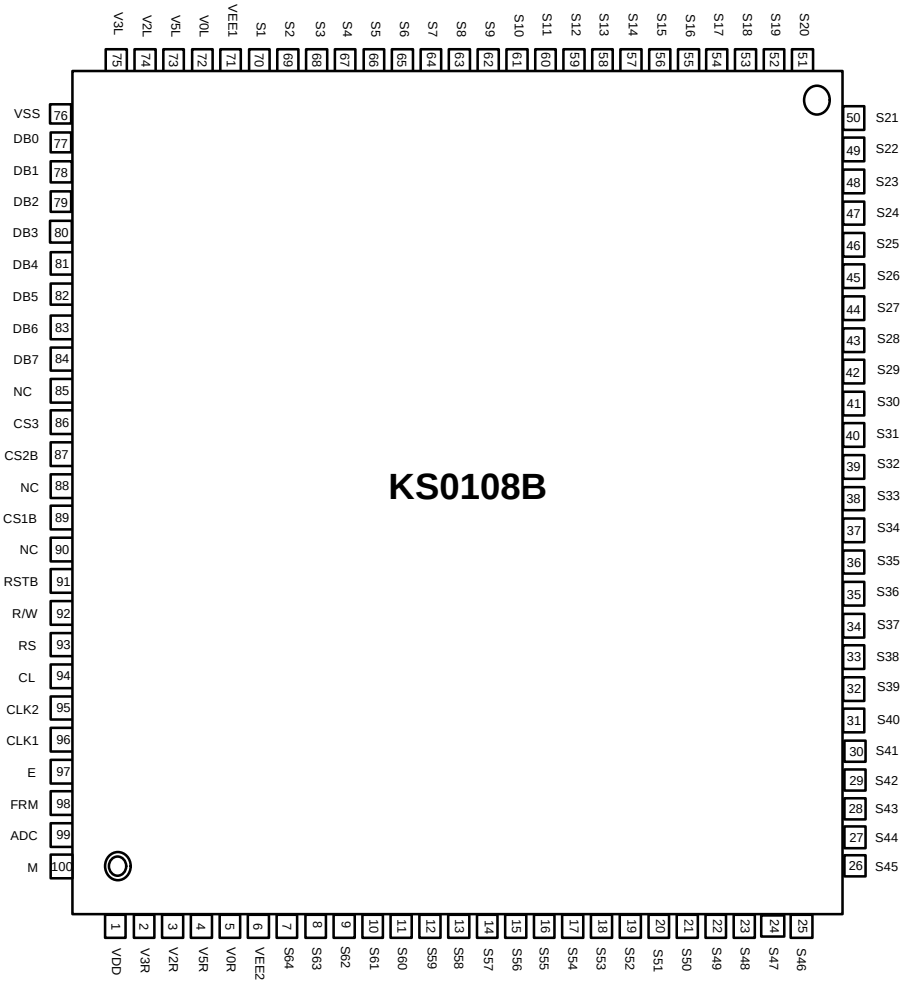
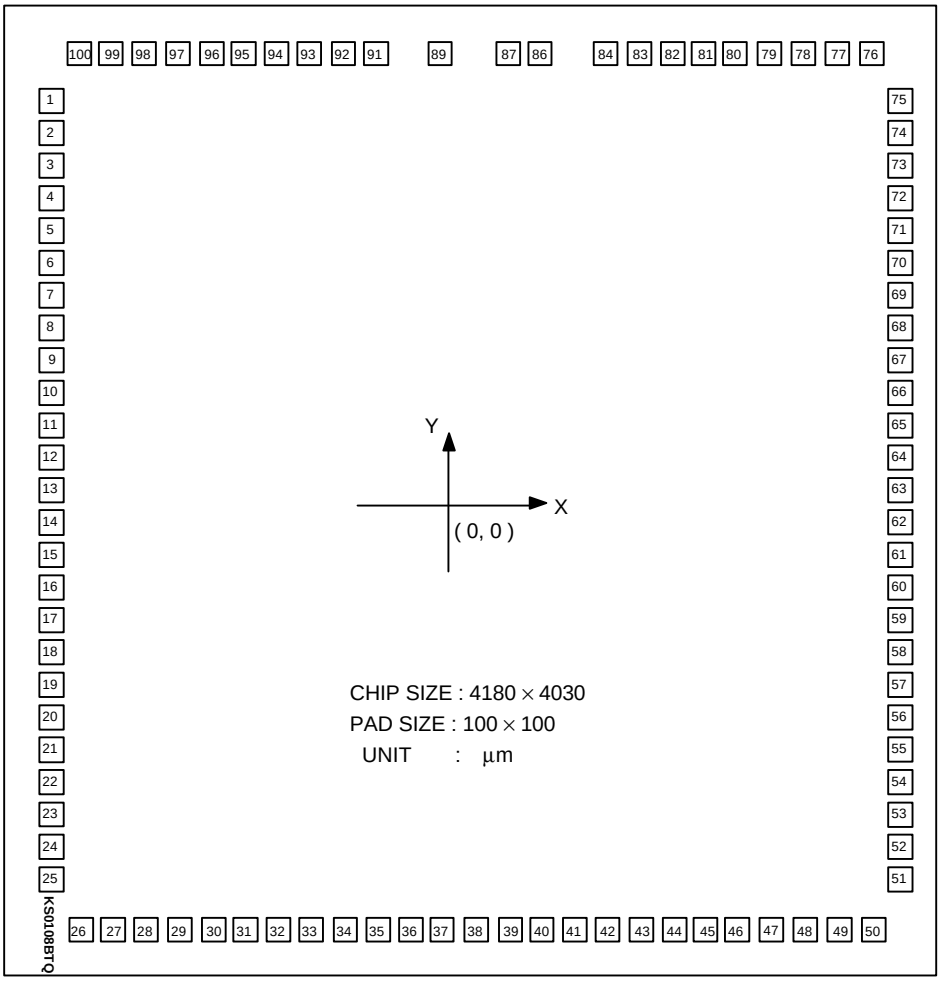


Fig3. 100TQFP Top View

PAD DIAGRAM (Chip Layout for the 100TQFP)



* There is mark of “KS0108BTQ” on the bottom left in the chip.

PAD LOCATION (100TQFP)

UNIT (μm)

PAD N/O	PAD NAME	COORDINATE		PAD N/O	PAD NAME	COORDINATE		PAD N/O	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
1	VDD	-1924	1812.5	41	S30	334.9	-1849	81	DB4	795.5	1849
2	V3R	-1924	1687.5	42	S29	462.1	-1849	82	DB5	670.5	1849
3	V2R	-1924	1562.5	43	S28	589.3	-1849	83	DB6	545.5	1849
4	V5R	-1924	1437.5	44	S27	716.5	-1849	84	DB7	420.5	1849
5	V0R	-1924	1312.5	45	S26	843.7	-1849	85	NC		
6	VEE2	-1924	1187.5	46	S25	970.9	-1849	86	CS3	282.8	1849
7	S64	-1924	1033.2	47	S24	1098.1	-1849	87	CS2B	157.8	1849
8	S63	-1924	906	48	S23	1225.3	-1849	88	NC		
9	S62	-1924	778.8	49	S22	1352.5	-1849	89	CS1B	32.8	1849
10	S61	-1924	651.6	50	S21	1479.7	-1849	90	NC		
11	S60	-1924	524.4	51	S20	1924	-1245.3	91	RSTB	-92.2	1849
12	S59	-1924	397.2	52	S19	1924	-1118.1	92	R/W	-217.2	1849
13	S58	-1924	270	53	S18	1924	-990.9	93	RS	-342.2	1849
14	S57	-1924	142.8	54	S17	1924	-863.7	94	CL	-467.2	1849
15	S56	-1924	15.6	55	S16	1924	-736.5	95	CLK2	-592.2	1849
16	S55	-1924	-111.6	56	S15	1924	-609.3	96	CLK1	-717.2	1849
17	S54	-1924	-238.8	57	S14	1924	-482.1	97	E	-842.2	1849
18	S53	-1924	-366	58	S13	1924	-354.9	98	FRW	-967.2	1849
19	S52	-1924	-493.2	59	S12	1924	-227.7	99	ADC	-1177.8	1849
20	S51	-1924	-620.4	60	S11	1924	-100.5	100	M	-1312.8	1849
21	S50	-1924	-747.6	61	S10	1924	26.7				
22	S49	-1924	-874.8	62	S9	1924	153.9				
23	S48	-1924	-1002	63	S8	1924	281.1				
24	S47	-1924	-1129.2	64	S7	1924	408.3				
25	S46	-1924	-1256.4	65	S6	1924	535.5				
26	S45	-1573.1	-1849	66	S5	1924	662.7				
27	S44	-1445.9	-1849	67	S4	1924	789.9				
28	S43	-1318.7	-1849	68	S3	1924	917.1				
29	S42	-1191.5	-1849	69	S2	1924	1044.3				
30	S41	-1064.3	-1849	70	S1	1924	1171.5				
31	S40	-937.1	-1849	71	VEE1	1924	1312.5				
32	S39	-809.9	-1849	72	V0L	1924	1437.5				
33	S38	-682.7	-1849	73	V5L	1924	1562.5				
34	S37	-555.5	-1849	74	V2L	1924	1687.5				
35	S36	-428.3	-1849	75	V3L	1924	1812.5				
36	S35	-301.1	-1849	76	VSS	1450.5	1849				
37	S34	-173.9	-1849	77	DB0	1315.5	1849				
38	S33	-46.7	-1849	78	DB1	1180.5	1849				
39	S32	80.5	-1849	79	DB2	1045.5	1849				
40	S31	207.7	-1849	80	DB3	920.5	1849				

PIN DESCRIPTION

PIN NUM QFP(TQFP)	SYMBOL	INPUT/OUTPUT	DESCRIPTION
3(1) 78(76) 73(71), 8(6)	V_{DD} V_{SS} $V_{EE1.2}$	Power	For internal logic circuit (+5V ± 10%) GND (0V) For LCD driver circuit V_{SS}=0V, V_{DD}=+5V ±10% , V_{DD}-V_{EE}=8V~17V V_{EE1} and V_{EE2} is connected by the same voltage.
74(72), 7(5) 76(74), 5(3) 77(75), 4(2) 75(73), 6(4)	V0L, V0R V2L, V2R V3L, V3R V5L, V5R	Power	Bias supply voltage terminals to drive the LCD. Select Level: V0L(R), V5L(R) / Non-Select Level: V2L(R), V3L(R) V0L and V0R (V2L & V2R, V3L & V3R, V5L & V5R) should be connected by the same voltage.
92(90) 91(89) 90(88)	CS1B CS2B CS3	Input	Chip selection In order to interface data for input or output, the terminals have to be CS1B=L, CS2B=L, and CS3=H.
2(100)	M	Input	Alternating signal input for LCD driving.
1(99)	ADC	Input	Address control signal to determine the relation between Y address of display RAM and terminals from which the data is output. ADC=H→ Y0:S1 ~ Y63:S64 ADC=L→ Y0:S64 ~ Y63:S1
100(98)	FRM	Input	Synchronous control signal. Presets the 6-bit Z counter and synchronizes the common signal with the frame signal when the frame signal becomes high.
99(97)	E	Input	Enable signal. write mode (R/W=L) → data of DB<0:7> is latched at the falling edge of E. read mode (R/W=H) → DB<0:7> appears the reading data while E is at high level.
98(96) 97(95)	CLK1 CLK2	Input	2 phase clock signal for internal operation. Used to execute operations for input/output of display RAM data and others.
96(94)	CL	Input	Display synchronous signal. Display data is latched at rising time of the CL signal and increments the Z-address counter at the CL falling time.
95(93)	RS	Input	Data or Instruction. RS=H→DB<0:7> : Display RAM Data RS=L→DB<0:7> : Instruction Data
94(92)	R/W	Input	Read or Write. R/W=H → Data appears at DB<0:7> and can be read by the CPU while E=H, CS1B=L, CS2B=L and CS3=H. R/W=L→Display data DB<0:7> can be written at falling of E when CS1B=L, CS2B=L and CS3=H.
79~86 (77~84)	DB0~DB7	Input/Output	Data bus. There state I/O common terminal.

PIN DESCRIPTION (continued)

<table>
<tr><th>PIN NUM
QFP(TQFP)</th><th>NAME</th><th>INPUT/OUTPUT</th><th>DESCRIPTION</th></tr>
<tr><td>72~9
(70~7)</td><td>S1~S64</td><td>Output</td><td>LCD Segment driver output.
Display RAM data 1:ON
Display RAM data 0:OFF
(Relation of display RAM data & M)
<table>
<tr><th>M</th><th>DATA</th><th>Output Level</th></tr>
<tr><td rowspan="2">L</td><td>L</td><td>V_2</td></tr>
<tr><td>H</td><td>V_0</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td>V_3</td></tr>
<tr><td>H</td><td>V_5</td></tr>
</table></td></tr>
<tr><td>93(91)</td><td>RSTB</td><td>Input</td><td>Reset signal.
When RSTB=L,
1) ON/OFF register becomes set by 0. (display off)
2) Display start line register becomes set by 0
(Z-address 0 set, display from line 0)
After releasing reset, this condition can be changed only by instruction.</td></tr>
<tr><td>87(85),88(88)
89(90)</td><td>NC</td><td></td><td>No connection.(open)</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating Voltage	V_{DD}	-0.3~+7.0	V	*1
Supply Voltage	V_{EE}	V_{DD}-19.0~V_{DD}+0.3	V	*4
Driver Supply Voltage	V_B	-0.3~V_{DD}+0.3	V	*1,3
	V_{LCD}	V_{EE}-0.3~V_{DD}+0.3	V	*2
Operating Temperature	T_{OPR}	-30~+85	°C	
Storage Temperature	T_{STG}	-55~+125	°C	

*1. Based on V_{SS}=0V.
*2. Applies the same supply voltage to V_{EE1} and V_{EE2}. V_{LCD}=V_{DD}-V_{EE}.
*3. Applies to M, FRM, CL, RSTB, ADC, CLK1, CLK2, CS1B, CS2B, CS3, E, R/W, RS and DB0~DB7.
*4. Applies to V0L(R), V2L(R), V3L(R) and V5L(R).
Voltage level: $V_{DD} \geq$ V0L= V0R $\geq$ V2L= V2R $\geq$ V3L= V3R $\geq$ V5L= V5R $\geq V_{EE}$.

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD}=+5V ±10%, V_{SS}=0V, V_{DD}-V_{EE}=8~17V, T_a=-30~+85°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit	Note
Input High Voltage	V_{IH1}	-	0.7V_{DD}	-	V_{DD}	V	*1
	V_{IH2}	-	2.0	-	V_{DD}	V	*2
Input Low Voltage	V_{IL1}	-	0	-	0.3V_{DD}	V	*1
	V_{IL2}	-	0	-	0.8	V	*2
Output High Voltage	V_{OH}	I_{OH}=-200μA	2.4	-	-	V	*3
Output Low Voltage	V_{OL}	I_{OL}=1.6mA	-	-	0.4	V	*3
Input Leakage Current	I_{LKG}	V_{IN}=V_{SS}~V_{DD}	-1.0	-	1.0	μA	*4
Three-state(OFF) Input Current	I_{TSL}	V_{IN}=V_{SS}~V_{DD}	-5.0	-	5.0	μA	*5
Driver Input Leakage Current	I_{DIL}	V_{IN}=V_{EE}~V_{DD}	-2.0	-	2.0	μA	*6
Operating Current	I_{DD1}	During Display	-	-	100	μA	*7
	I_{DD2}	During Access Access Cycle=1MHz	-	-	500	μA	*7
On Resistance	R_{ON}	V_{DD}-V_{EE}=15V I_{LOAD}= ± 0.1mA	-	-	7.5	KΩ	*8

*1. CL, FRM, M, RSTB, CLK1, CLK2
*2. CS1B, CS2B, CS3, E, R/W, RS, DB0~DB7
*3. DB0~DB7
*4. Except DB0~DB7
*5. DB0~DB7 at High Impedance
*6. V0L(R), V2L(R), V3L(R), V5L(R)
*7. 1/64 duty, FCLK=250KHZ, Frame Frequency=70HZ, Output: No Load
*8. V_{DD}~V_{EE}=15.5V
V0L(R)>V2L(R)=V_{DD}-2/7 (V_{DD}-V_{EE})>V3L(R)=V_{EE}+2/7(V_{DD}-V_{EE})>V5L(R)

AC Characteristics (V_{DD}=+5V ±10%, V_{SS}=0V, T_a=-30°C~+85°C)

1. Clock Timing

Characteristic	Symbol	Min	Typ	Max	Unit
CLK1, CLK2 Cycle Time	t_{CY}	2.5	-	20	µs
CLK1 'LOW' Level Width	t_{WL1}	625	-	-	ns
CLK2 'LOW' Level Width	t_{WL2}	625	-	-	
CLK1 'HIGH' Level Width	t_{WH1}	1875	-	-	
CLK2 'HIGH' Level Width	t_{WH2}	1875	-	-	
CLK1-CLK2 Phase Difference	t_{D12}	625	-	-	
CLK2-CLK1 Phase Difference	t_{D21}	625	-	-	
CLK1, CLK2 Rise Time	t_R	-	-	150	
CLK1, CLK2 Fall Time	t_F	-	-	150	

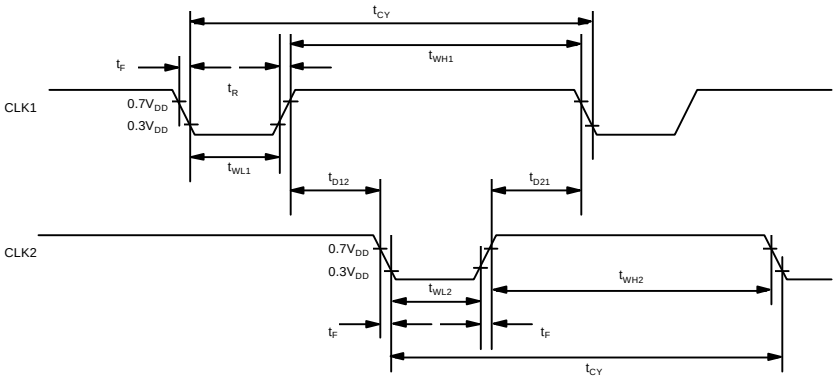


Fig4. External clock waveform

2. Display Control Timing

Characteristic	Symbol	Min	Typ	Max	Unit
FRM Delay Time	t_{DF}	-2	-	+2	us
M Delay Time	t_{DM}	-2	-	+2	us
CL 'LOW' Level Width	t_{WL}	35	-	-	us
CL 'HIGH' Level Width	t_{WH}	35	-	-	us

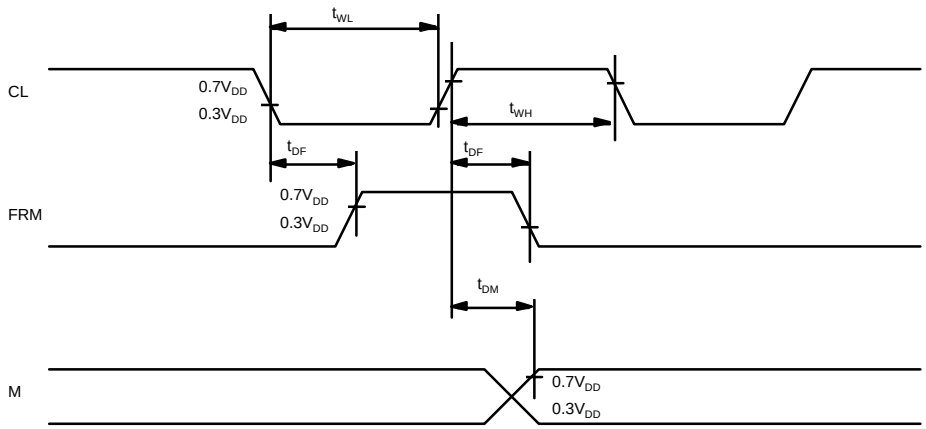


Fig 5. Display control signal waveform

3. MPU Interface

Characteristic	Symbol	Min	Typ	Max	Unit
E Cycle	t_C	1000	-	-	ns
E High Level Width	t_{WH}	450	-	-	ns
E Low Level Width	t_{WL}	450	-	-	ns
E Rise Time	t_R	-	-	25	ns
E Fall Time	t_F	-	-	25	ns
Address Set-Up Time	t_{ASU}	140	-	-	ns
Address Hold Time	t_{AH}	10	-	-	ns
Data Set-Up Time	t_{DSU}	200	-	-	ns
Data Delay Time	t_D	-	-	320	ns
Data Hold Time (Write)	t_{DHW}	10	-	-	ns
Data Hold Time (Read)	t_{DHR}	20	-	-	ns

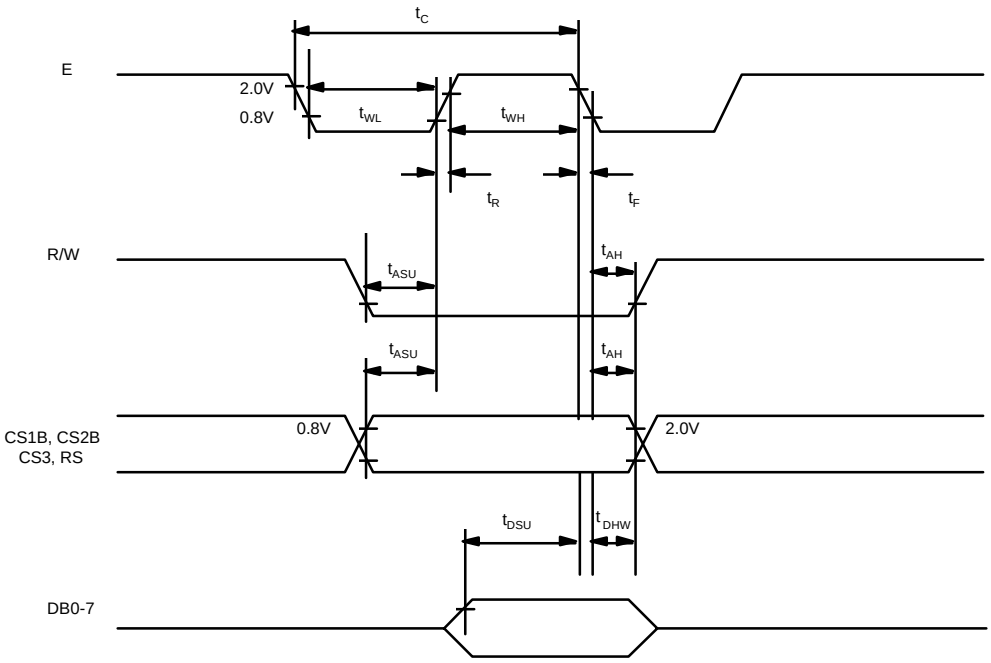


Fig 6. MPU write timing

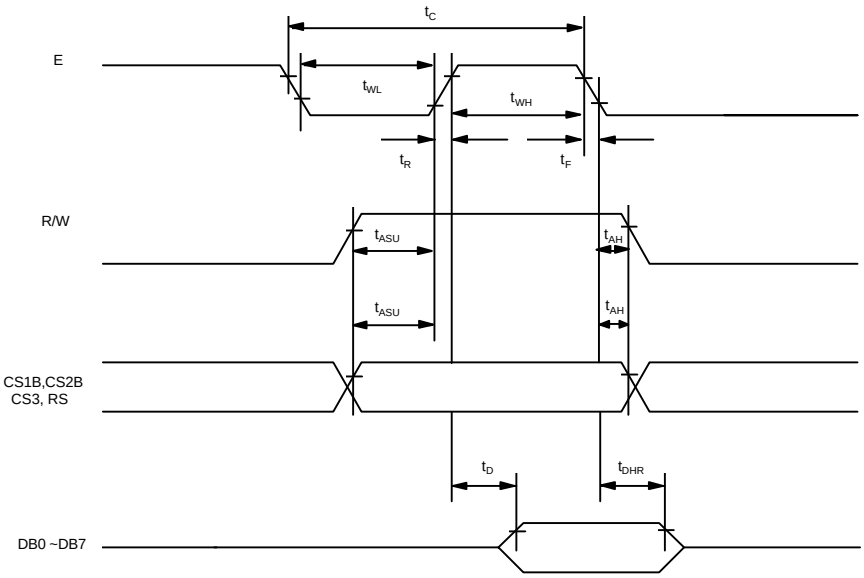


Fig 7. MPU Read timing

OPERATING PRINCIPLES & METHODS

1. I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

2. Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.

When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then Writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

3. Output register

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H, RS=L, status data (busy check) can read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

4. Reset

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.

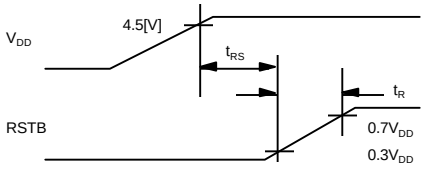
1. Display off
2. Display start line register become set by 0.(Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4=0 (clear RSTB) and DB7=0 (ready) by status read instruction.

The Conditions of power supply at initial power up are shown in table 1.

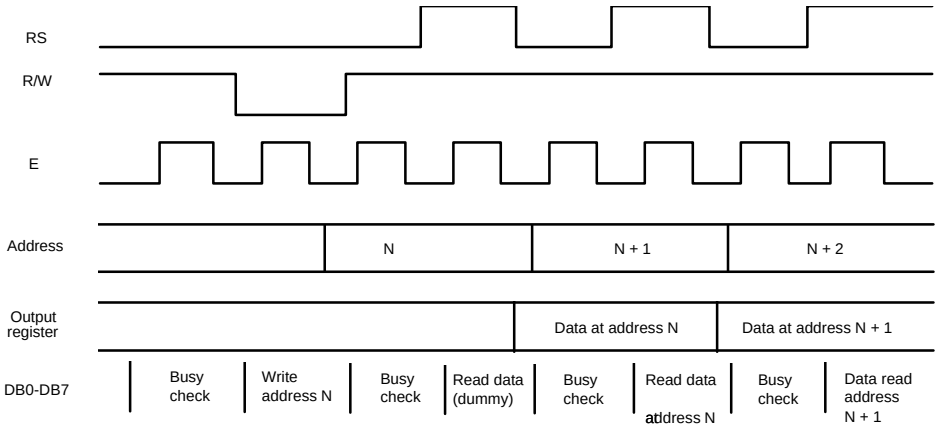
Table 1. Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	-	-	us
Rise Time	t_R	-	-	200	ns

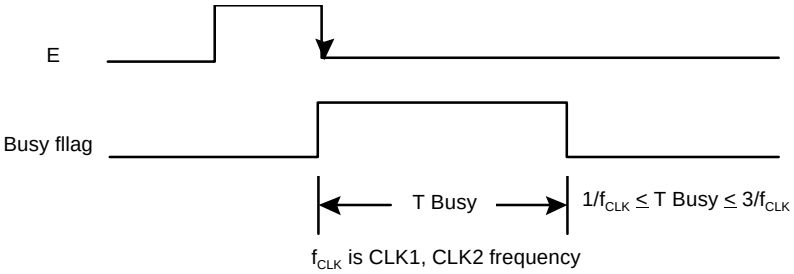


5. Busy flag

Busy flag indicates that KS0108B is operating or no operating. When busy flag is high, KS0108B is in internal operating.
When busy flag is low, KS0108B can accept the data or instruction.
DB7 indicates busy flag of the KS0108B.



Busy Check



Busy Flag

6. Display On/Off Flip - Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data.

The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low.

The status of the flip-flop is output to DB5 by status read instruction.

The display on/off flip-flop synchronized by CL signal.

7. X Page Register

X page register designates pages of the internal display data RAM.

Count function is not available. An address is set by instruction.

8. Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

9. Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write data 1. The other way, off state, writes 0.

Display data RAM address and segment output can be controlled by ADC signal.

ADC=H⇒ Y-address 0:S1 ~ Y address 63:S64

ADC=L⇒ Y-address 0:S64 ~ Y address 63:S1

ADC terminal connect the V_{DD} or V_{SS}.

10. Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display.

Bit data (DB<0:5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.

It is used for scrolling of the liquid crystal display screen.

DISPLAY CONTROL INSTRUCTION

The display control instructions control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display ON/OFF	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON
Set Address (Y address)	L	L	L	H	Y address (0~63)						Sets the Y address in the Y address counter.
Set Page (X address)	L	L	H	L	H	H	H	Page (0~7)			Sets the X address at the X address register.
Display Start Line (Z address)	L	L	H	H	Display start line (0~63)						Indicates the display data RAM displayed at the top of the screen.
Status Read	L	H	BUSY	L	ON/OFF	RESET	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Write Display Data	H	L	Write Data								Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read Display Data	H	H	Read Data								Reads data (DB0:7) from display data RAM to the data bus.

1. Display On/Off

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0.
Though the data is not on the screen with D=0, it remains in the display data RAM.
Therefore, you can make it appear by changing D=0 into D=1.

2. Set Address (Y Address)

S	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0 ~ AC5) of the display data RAM is set in the Y address counter.
An address is set by instruction and increased by 1 automatically by read or write operations of display data.

3. Set Page (X Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

X address(AC0 ~ AC2) of the display data RAM is set in the X address register.
Writing or reading to or from MPU is executed in this specified page until the next page is set.

4. Display Start Line (Z Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

Z address (AC0 ~ AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen.
When the display duty cycle is 1/64 or others(1/32 ~ 1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

5. Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY
  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.
  When BUSY is 0, the Chip is ready to accept any instructions.
- ON/OFF
  When ON/OFF is 1, the display is on.
  When ON/OFF is 0, the display is off.
- RESET
  When RESET is 1, the system is being initialized.
  In this condition, no instructions except status read can be accepted.
  When RESET is 0, initializing has finished and the system is in the usual operation condition.

6. Write Display Data

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	D7	D6	D5	D4	D3	D2	D1	D0

Writes data (D0 ~ D7) into the display data RAM.
After writing instruction, Y address is increased by 1 automatically.

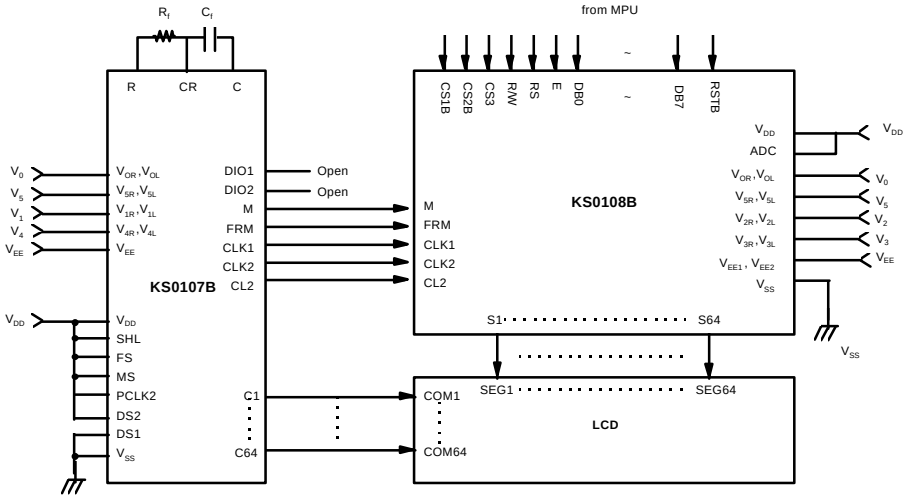
7. Read Display Data

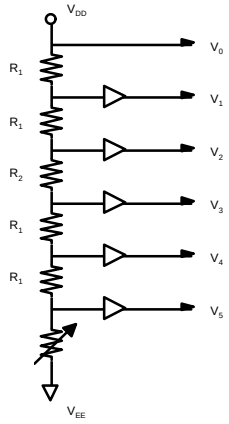
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Reads data (D0 ~ D7) from the display data RAM.
After reading instruction, Y address is increased by 1 automatically.

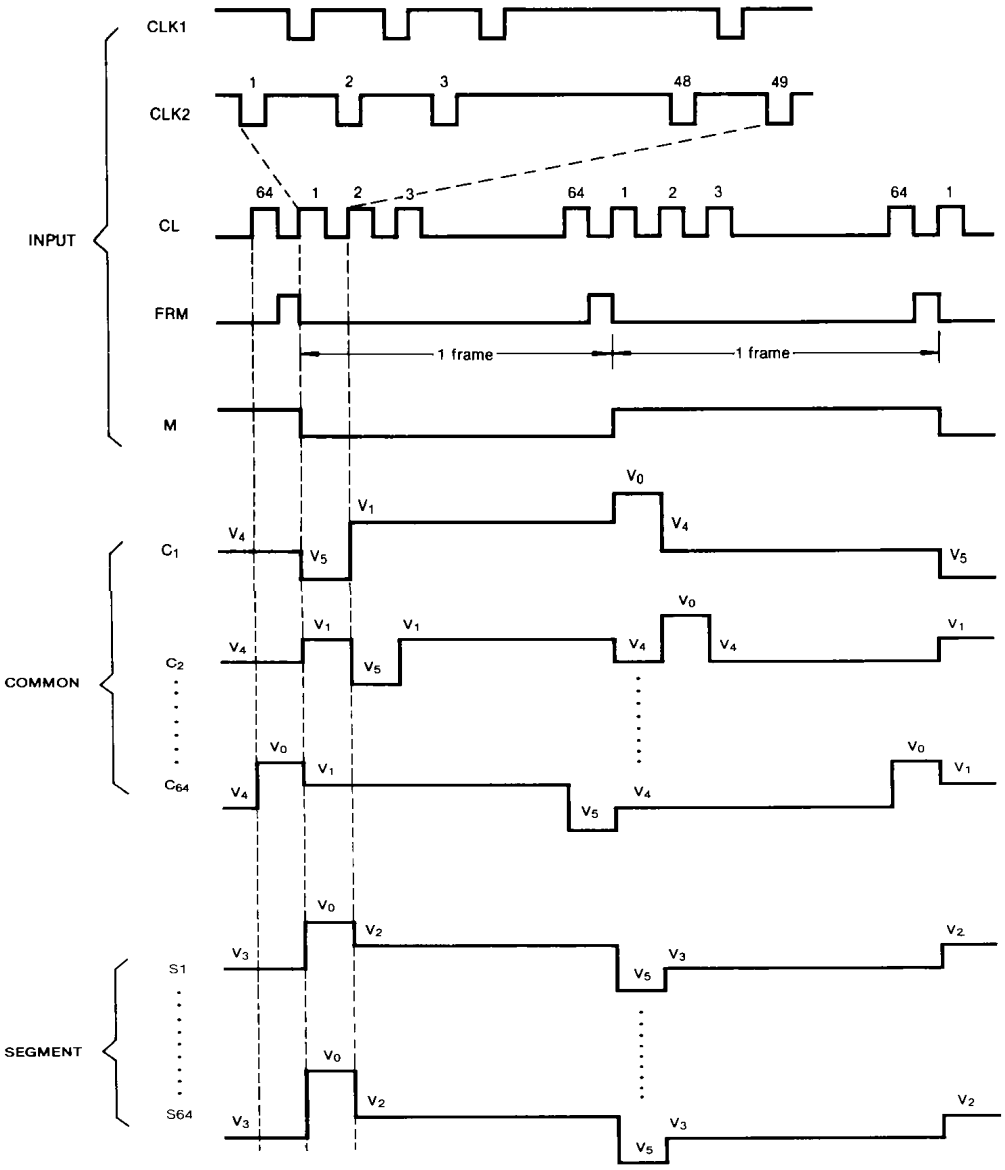
APPLICATION CIRCUIT

1.1/64 duty common driver(KS0107B) interface circuit





2. Timing diagram (1/64 duty)



3. LCD Panel interface application circuit